



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES

JPCA



IPC/JPCA-2315

Design Guide for High Density Interconnects (HDI) and Microvias

IPC/JPCA-2315

June 2000

A standard developed by IPC and JPCA

2215 Sanders Road, Northbrook, IL 60062-6135
Tel. 847.509.9700 Fax 847.509.9798
www.ipc.org

The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

IPC Position Statement on Specification Revision Change

It is the position of IPC's Technical Activities Executive Committee (TAEC) that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC standard/guideline is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision.
Adopted October 6, 1998

Why is there a charge for this standard?

Your purchase of this document contributes to the ongoing development of new and updated industry standards. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low in order to allow as many companies as possible to participate. Therefore, the standards revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit www.ipc.org or call 847/790-5372.

Thank you for your continued support.



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES

JPCA



IPC/JPCA-2315

Design Guide for High Density Interconnects (HDI) and Microvias

Developed by the High Density Interconnect (HDI) Design Subcommittee (D-41) of the High Density Interconnect (HDI) Committee (D-40) of IPC and the Build-Up PWB Committee of the Japan Printed Circuit Association (JPCA)

IPC Standards and Artificial Intelligence (AI) Statement – 2025

IPC explicitly prohibits:

- The integration or transfer of any data whether in the form of IPC books, standards, metadata, or other formats — into AI engines or algorithms by any person or entity, including authorized distributors and their end users.
- Activities involving data harvesting, text and data mining, enrichment, or the creation of derivative works based on this data, including the use of automated data collection methods or artificial intelligence.

Any breach of these provisions is considered a copyright infringement unless expressly and formally authorized by IPC.

Users of this standard are encouraged to participate in the development of future revisions.

Contact:

IPC
2215 Sanders Road
Northbrook, Illinois
60062-6135
Tel 847 509.9700
Fax 847 509.9798

Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the High Density Interconnect (HDI) Design Subcommittee (D-41) of the High Density Interconnect (HDI) Committee (D-40) and the JPCA Build-Up PWB Committee are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC and JPCA extend their gratitude.

High Density Interconnect (HDI) Committee

Chairman
Bob Neves
Microtek Laboratories

High Density Interconnect (HDI) Design Subcommittee

Chairman
Lionel Fullwood
WKK Distribution Ltd.

Technical Liaisons of the IPC Board of Directors

Stan Plzak	Peter Bigelow
Pensar Corp.	Beaver Brook
	Circuits Inc.

JPCA Build-Up PWB Committee

Chairman
Kanji Ohtsuka
Meisei University

JPCA Build-Up PWB Committee

Secretary
Setsuo Noguchi
NEC Toyama, Ltd.

High Density Interconnect (HDI) Design Subcommittee

David R Backen, Honeywell
Advanced Circuits, Inc.
Steve Bakke, C.I.D., Alliant
Techsystems Inc.
Scott Ballard, Lockheed Martin
Space Systems,
Richard W. Barry, Austria
Technologie & Systemtechnik AG
Mark A. Bosnjak, Carolina Circuits
Co.
Larry W. Burgess, MicroPak
Laboratories, Inc.
Lewis Burnett, Honeywell, Inc.
Dennis J. Cantwell, Printed Circuits,
Inc.
Marc Carter, Chemelex Division-RBP
Chemical Corp.
Byron Case, L-3 Communications
Ignatius Chong, Celestica
International, Inc.
David A. Chopourian, Printed Circuit
Corp.
Christine R. Coapman, Delphi Delco
Electronics Systems
Robert Cole, Rogers Corp.
David J. Corbett, Defense Supply
Center Columbus
Charles Dal Currier, Ambitech, Inc.
Donna Dearing, Honeywell
Advanced Circuits, Inc.
John F. DeBrita, Sanmina Corp.

John Devine, Cabletron Systems, Inc.
Joseph A. DiPalermo, Parlex Corp.
C. Don Dupriest, Lockheed Martin
John Dusi, Lockheed Martin
SMS & S
Werner Engelmaier, Engelmaier
Associates, L.C.
Michael C. Fitts, The Solution Fitts
Dennis Fritz, MacDermid, Inc.
Lionel Fullwood, WKK Distribution
Ltd.
Rolf E. Funer, Funer Associates
Thomas F. Gardeski, E. I. du Pont de
Nemours and Co.
William J. Gebhardt, C.I.D.
Pete Gilmore, Shipley Ronal
Paul Grande, Jr., U.S. Navy
Richard T. Grannells, United
Technologies
Foster L. Gray, PC Interconnects
Michael R. Green, Lockheed Martin
Space Systems
Don Gustafson, Olec Corp.
Romella Hall, Rexam Custom
Mike Hassebrock, Rockwell Collins
Kazuo Hirasaka, Eastern Company
Ltd.
Happy T. Holden, Westwood
Associates
Robert Hubbard, Medtronic Inc./
Micro-Rel Division

Gerry Knoch, Atotech Deutschland
GmbH.
George T. Kotecki, Northrop
Grumman Corp.
Steve Liang, Conexant Systems, Inc.
Even Liu, Compeq Manufacturing
Co., Ltd.
Michael Lu, Compeq Manufacturing
Co., Ltd.
Michael G. Luke, C.I.D., Raytheon
Systems Co.
Curtis A. Lustig, Shipley Ronal
James F. Maguire, Intel Corp.
Wesley R. Malewicz, Siemens
Medical Systems, Inc.
John C Mather, Rockwell Collins
Dr. Goran Matijasevic, Ormet Corp.
Brian McDermott, Dynamic Details,
Inc.
Hue Morris, Lockheed Martin Space
Systems,
John H. Morton, C.I.D., Lockheed
Martin Corp.
Cameron T. Murray, 3M Co.
Sabine Neumann, Atotech
Deutschland GmbH.
David Nicol, Lucent Technologies,
Inc.
Benny Nilsson, Ericsson Radio
Systems AB
Steven M. Nolan, C.I.D., Silicon
Graphics Computer System

Deepak K. Pai, C.I.D., General
Dynamics Information Systems,
Inc.
Leticia Pinon-Zieren, DY 4 Systems,
Inc.
Jim R. Reed, Raytheon Systems Co.

Scott Sleeper, Medtronic Inc./
Micro-Rel Division
Thomas H Stearns, Brander
International Consultants
David A. Vaughan, Taiyo America,
Inc.

Bill Wike, IBM Corp.
John E. Williams, Raytheon Co.
David L. Wolf, Hadco Corp.
Thomas J Zanatta, Symbol
Technologies, Inc.
Sarah Zarrin, Seagate Technology

JPCA Build-Up PWB Committee

Yoshitaka Fukuoka, Toshiba Corp.
Kouji Ikawa, CMK Circuit
Technology Center Corp.
Tetsuro Irino, Hitachi Chemical Co.,
Ltd.
Satoshi Itaya, Oki Electric Industry
Co., Ltd.

Shogo Mizumoto, IBM Japan, Ltd.
Toshio Nakamura, Airex, Inc.
Yasuharu Nojima, Chiba Specialty
Chemicals K.K. Yoshizumi Satoh,
Toshiba Corp.
Kazuaki Shiraishi, Matsushita
Electronic Components Co., Ltd.

Tadashi Takai, Motorola Japan, Ltd.
Yoshinori Takazaki, Ividen Co.,
Ltd.
Eiji Takehara, Taiyo Ink Mfg. Co.,
Ltd.

This Page Intentionally Left Blank

Table of Contents

1 SCOPE	1	7 CLASSIFICATION OF PRODUCTS	19
1.1 Introduction	1	7.1 Structure.....	19
1.2 General.....	1	7.1.1 HDI Type I Constructions – 1[C]0 or 1[C]1	19
1.3 HDI Design Selection Guideline	1	7.1.2 HDI Type II Constructions – 1[C]0 or 1[C]1	19
1.4 Design Figures.....	1	7.1.3 HDI Type III Constructions – $\geq 2[C] \geq 0$	20
2 APPLICABLE DOCUMENTS	1	7.1.4 HDI Type IV Constructions – $>[P]0$	20
3 TERMS AND DEFINITIONS	1	7.1.5 Type V Constructions (Coreless) - Using Layer Pairs.....	20
3.1.1 Capture Land.....	1	7.1.6 Type VI Constructions	21
3.1.2 Target Land.....	1	7.2 Producibility	22
3.1.3 Stacked Vias	1	7.3 General Design Rules for Other HDI Constructions.....	23
3.1.4 Stacked Microvia.....	1	7.3.1 Staggered Via	23
4 MICROVIAS	1	7.3.2 Via-In-Land	24
4.1 Via Formation.....	2	7.4 Alternative Construction HDI Design Rules.....	24
4.1.1 Laser Ablated Vias	2	7.4.1 Variable Depth Microvias	24
4.1.2 Wet/Dry Etched Vias.....	3	7.4.2 Staggered Microvias.....	25
4.1.3 Photodielectric Vias.....	4	7.4.3 Co-Lamination with Conductive Paste.....	25
4.1.4 Conductive Inks/Insulation Displacement	4	7.4.4 Conductive Ink Sequential Buildup.....	25
4.1.5 Process Flow for Via Formation.....	4		
5 DENSITY EVALUATION	6		
5.1 Routability Prediction Methods	6		
5.1.1 Substrate Wiring Capacity Analysis	6		
5.1.2 Wiring Capacity (W_c)	6		
5.2 Design Basics.....	6		
5.3 Determining the Number of Conductors.....	7		
5.4 Wiring Factor (W_f).....	7		
5.4.1 Localized Escape Calculations	10		
5.4.2 Wiring Between Tightly Linked Components.....	11		
5.4.3 Total Wiring Requirements	12		
5.5 Via and Land Density	12		
5.6 Trade Off Process	12		
5.6.1 Wiring Factor Process	12		
5.6.2 Input/Output (I/O) Variables	12		
5.7 Typical Examples	12		
5.7.1 Case I – HDI With Direct Chip Attach.....	13		
5.7.2 Case II – Drilled Blind Via With SMT.....	15		
5.7.3 CASE III – Fine Pitch SMT.....	17		
5.7.4 Compare Alternatives.....	18		
5.8 Trade Off Worksheets	18		
6 MATERIALS	19		
6.1 Designation System.....	19		
6.2 Application Level.....	19		

Figures

Figure 1-1	Color Key	1
Figure 4-1	Cross Section of a General HDI with Microvias	2
Figure 4-2	Microvia Manufacturing Processes.....	2
Figure 4-3	Cross-Sectional Views of Methods to Make HDI with Microvias	3
Figure 4-4	Four Typical Constructions that Employ Lasers for Via Generation.....	3
Figure 4-5	Four Typical Constructions Utilizing Etched or Mechanically Formed Vias	4
Figure 4-6	Four Commercially Produced PID Boards	4
Figure 4-7	Four New HDI Boards that Employ Conductive Pastes as Vias.....	5
Figure 4-8	Summary of the Manufacturing Processes for PIDs, Laser, and Plasma Methods of Via Generation.....	5
Figure 5-1	Package Size and I/O Count.....	6
Figure 5-2	Feature Pitch and Feature Size Defining Channel Width	7
Figure 5-3	Channel Width Based on Conductors/Channel.....	8
Figure 5-4	One Conductor/Channel Feature Pitches	8
Figure 5-5	Conductors vs. Conductor Width – 2.5 mm [0.0984 in] Feature Pitch and 1.25 mm [0.04921 in] Land Width (Through-Hole Component)	8

Figure 5-6	Conductor vs. Conductor Width – 1.25 mm [0.04921 in] Feature Pitch and 0.15 mm [0.00591 in] Land Width	9
Figure 5-7	Conductor vs. Conductor Width – 0.65 mm [0.0256 in] Feature Pitch and 0.25 mm [0.00984 in] Land Width	9
Figure 5-8	Conductor vs. Conductor Width – 0.50 mm [0.0197 in] Feature Pitch and 0.125 mm [0.004921 in] Land Width	9
Figure 5-9	Wiring Factor Model for Tightly Coupled Components.....	12
Figure 5-10	Wiring Process Flow Chart.....	13
Figure 5-11	Typical Example of HDI with Direct Chip Attach	13
Figure 5-12	Example of Drilled Blind Via With SMT.....	15
Figure 5-13	Example of Fine Pitch SMT.....	17
Figure 7-1	Type I HDI Construction	20
Figure 7-2	Type II HDI Construction	22
Figure 7-3	Type III HDI Construction	22
Figure 7-4	Design Example for Type III HDI with Stacked Microvias	23
Figure 7-5	Design Example for Type III HDI with Staggered Microvias	23
Figure 7-6	Type IV HDI Construction.....	24
Figure 7-7	Coreless Type V HDI Construction.....	24
Figure 7-8	Type VI Construction	24
Figure 7-9	Staggered Vias	25
Figure 7-10	Via-In-Land Design Example.....	25
Figure 7-11	Design Example for HDI Board with Variable Depth Microvias	26
Figure 7-12	Design Example for HDI Board with Staggered Microvias	26
Figure 7-13	Design Example for HDI Board Co- Laminated with Conductive Paste	27
Figure 7-14	Design Example for HDI Board Utilizing Conductive Ink Build Up	27

Tables

Table 5-1	Number of Conductors for Gridded Router When Feature Pitch is 2.5 mm [0.0983 in]	9
Table 5-2	Number of Conductors for Gridded Router When Feature Pitch is 1.25 mm [0.04921 in]	10
Table 5-3	Number of Conductors for Gridded Router When Feature Pitch is 0.65 mm [0.0256 in]	10
Table 5-4	Number of Conductors for Gridded Router When Feature Pitch is 0.50 mm [0.0197 in]	10
Table 5-5	Number of Conductors for Gridded Router When Feature Pitch is 0.25 mm [0.00984 in]	10
Table 5-6	Pad Rows that can Escape per HDI Layer for Different Feature Sizes	11
Table 5-7	Efficiencies	13
Table 5-8	Conductors Per Channel (Two Conductors; Assumes 0.03 cm [0.012 in] Land Size).....	14
Table 5-9	Number of Conductors Per Channel (Two Conductors; Assumes 0.020 cm [0.00787 in] Land Size)	15
Table 5-10	Advanced Design Rules (Assumes 0.027 cm [0.010630 in] Land Size).....	15
Table 5-11	Advanced Technology Substrate Alternative.....	15
Table 5-12	Total Layer Counts and Alternatives	16
Table 5-13	Design Alternatives Based on Layers, Vias, and Design Rules.....	16
Table 5-14	Reporting Requirements Example HDI PWBs with Blind Vias.....	16
Table 5-16	Advanced Technology Alternatives	
Table 5-15	Conventional Technology Board Reporting Requirements Example	18
Table 7-1	Typical Feature Sizes for HDI Constructions.....	21
Table 7-2	Conductive Paste Co-Lamination Design Rules	25