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This Standard does not purport to address all safety problems associated with its use or all applicable regulatory requirements. It is the responsibility of the user of this Standard to establish appropriate safety and health practices and to determine the applicability of regulatory limitations before its use.

(From Standards Proposal No. 5524 formulated under the cognizance of the EIA S-1 Passive Component Steering Committee).

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FIGURES

TABLES

1 SCOPE

This industry standard outlines typical worst case industry printed wiring board (PWB) assembly process conditions for passive and solid state electronic devices (hereafter referred to as "devices). This standard provides evaluation procedures to determine whether a device can be safely subjected to those PWB assembly processes and still meet all device specifications and reliability and quality expectations. This standard provides a methodology to classify any limitation identified by the evaluation procedures in this document in order to convey to the electronics industry a singular format for providing process limitation information to PWB assemblers and OEMs that will allow them to develop PWB assembly processes that will not exceed any documented device limitations. This standard **shall** not be used to evaluate sockets and connectors, instead reference EIA 364-56 and EIA 364-61.

The classification requirements of this document are required for passive devices.

Any surface mountable, solid state device that has been classified per J-STD-020 using the appropriate thermal profile in J-STD-020 based on its package dimensions is not required to be classified per this standard for thermal limitations. Similarly, any through hole mounted, solid state device that meets the requirements of JESD22-B106 is not required to be classified per this standard for thermal limitations. However, any solid state device that has a history of thermal limitations or may have limitations to X-ray exposure, common PWB cleaning operations, or other commonly performed assembly processes is strongly recommended to be classified for those process limitations per this standard. Surface mounted, solid state devices **shall** not be classified to the wave solder process stated in this standard.

The solder assembly process conditions listed in this document are not recommended conditions for an assembler. An assembler needs to consider many factors when establishing a safe assembly process for a given printed wiring board (PWB) assembly. This standard outlines a process to classify and label an electronic device's Process Sensitivity Level (PSL) and Moisture Sensitivity Level (MSL) consistent with the semiconductor industry's classification levels.

This standard does not establish re-work simulation conditions. However, this document does highlight some commonly used alternate solder assembly processes used for attaching replacement devices. It is recommended that suppliers be aware of alternate attach processes if they are commonly used on their devices and determine if their devices are sensitive to the temperature values and durations of these alternate processes.

This standard provides temperature sensitivity classifications for devices attached by soldering processes using Sn/Ag/Cu (SAC) solders which may reach 260 °C and possibly higher. However, this standard can also be used to denote the temperature limitations of devices designed to be attached using solder alloys with lower process temperatures (e.g., low temperature solders (LTS) such as near eutectic SnBi). J-STD-020 has defined a classification temperature of 190 °C for LTS, thus any device designed to be attached using LTS that is not able to withstand the 190 °C peak reflow temperature requirement can be classified as process sensitive per this standard. See Example #8 in Annex A.