



**IPC-7095A**

# **Design and Assembly Process Implementation for BGAs**

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Users of this publication are encouraged to participate in the  
development of future revisions.

Contact:

IPC  
3000 Lakeside Drive, Suite 309S  
Bannockburn, Illinois  
60015-1219  
Tel 847 615.7100  
Fax 847 615.7105

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# Design and Assembly Process Implementation for BGAs

## 1 SCOPE

This document describes the design and assembly challenges for implementing Ball Grid Array (BGA) and Fine Pitch BGA (FBGA) technology. The effect of BGA and FBGA on current technology and component types is also addressed. The focus on the information contained herein is on critical inspection, repair, and reliability issues associated with BGAs.

**1.1 Purpose** The target audiences for this document are managers, design and process engineers, and operators and technicians who deal with the electronic assembly, inspection, and repair processes. The intent is to provide useful and practical information to those who are using BGAs and those who are considering BGA implementation.

**1.2 Selection Criteria (Determination of Package Style and Assembly Processes)** Every electronic system consists of various parts: interfaces, electronic storage media, and the printed board assembly. Typically, the complexity of these systems is reflected in both the type of components used and their interconnecting structure. The more complex the components, as judged by the amount of input/output terminals they possess, the more complex is the interconnecting substrate.

Cost and performance drivers have resulted in increased component density, and a greater number of components attached to a single assembly, while the available mounting real estate has shrunk. In addition, the number of functions per device has increased and this is accommodated by using increased I/O count and reduced contact pitch. Reduced contact pitch represents challenges for both assemblers and bare board manufacturers. Assemblers encounter handling, coplanarity and alignment problems.

The board manufacturers must deal with land size issues, solder mask resolution and electrical test problems.

Based on industry predictions one would believe that all component packages have over 200 I/Os and are increasing in I/O count. Actually, components with the highest usage have I/O counts in the 16 to 64 I/O range. Over 50% of all components fall into this category, while only 5% of all components used have over 208 I/Os, which may be the threshold for determining the cross-over point between peripheral leaded component style packages and array type formats.

Many peripherally leaded, lower I/O count devices, such as memory and logic devices, are being converted to area array packaging formats as either BGAs or Fine Pitch BGAs.

Although the percentage of high I/O components used on an electronic assembly is small, they play a big part in driving the industry infrastructure for both bare board and assembly manufacturing. These high I/O components determine the process for bare board imaging, etching, testing and surface finishing. They determine the materials used for fabrication and drive assembly process improvements in a similar manner.

The electronics industry has evolved from using through-hole assembly technology in which the component leads went into the printed board substrate and were either soldered to the bottom side of the board or into a plated-through hole. Surface Mounting Technology (SMT) has advanced to a stage where the majority of electronic components manufactured today are only available in SMT form.

Manufacturing products with SMT in any significant volume requires automation. For low volume, a manually operated machine or a single placement machine may be sufficient. High volume SMT manufacturing requires special solder paste deposition systems, multiple and various placement machines, in-line solder reflow systems and cleaning systems.

The heart of surface mount manufacturing is the machine that places the components onto the printed board land areas prior to soldering. Unlike through-hole (TH) insertion machines, surface mount placement machines are usually capable of placing many different component types. As design densities have increased, new SMT package styles have evolved. Examples are Fine Pitch Technology (FPT), Ultra Fine Pitch Technology (UFPT), and Array Surface Mount (ASM). This latter category consists of the many families of ball or column grid arrays and the chip scale packages (CSP) and Fine Pitch BGAs (FBGA). These parts are all capable of being placed by machines provided that the equipment has the required positioning accuracy.

Increased device complexity has been a primary driving factor for SMT. In order to minimize the component package size, component lead spacing has decreased (e.g., 1.27 mm to 0.65 mm). Further increases in semiconductor integration requiring more than 196 I/Os can drive packages to even closer perimeter lead spacing, such as 0.5 mm, 0.4 mm, 0.3 mm, and 0.25 mm. However, the array package format has become the favorite for high I/O count devices. Area array component package styles have a pitch that originally was much larger than the equivalent peripherally leaded device, however that lead format is now also seeing reductions in pitch configurations.