IPC/JEDEC-9703

Mechanical Shock Test Guidelines for Solder Joint Reliability

Developed by the JEDEC Reliability Test Methods for Packaged Devices Committee (JC-14.1) and the SMT Attachment Reliability Test Methods Task Group (6-10d) of the Product Reliability Committee (6-10) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois
60015-1219
Tel 847 615.7100
Fax 847 615.7105

Table of Contents

1 SCOPE ... 1

2 APPLICABLE DOCUMENTS ... 1

2.1 IPC ... 1

2.2 American Society for Testing and Materials ... 1

3 TERMS AND DEFINITIONS ... 1

4 USE CONDITIONS OVERVIEW ... 2

4.1 Scope and Application of UCs ... 2

4.2 Capturing UC Data ... 2

4.3 Methods for Developing UCs ... 2

4.3.1 Approach 1 – UC Derivation Approach ... 2

4.3.2 Approach 2 – Leveraging Existing Data to Usage Model ... 3

4.3.3 Torture Tests ... 3

5 SYSTEM TESTS ... 4

5.1 Shock Test Equipment ... 4

5.1.1 Drop Testers ... 4

5.1.2 Shock Machines ... 5

5.1.3 Inclined Impact ... 5

5.1.4 Fixturing ... 6

5.2 Correlation Criteria ... 6

5.2.1 Unpackaged System Input Correlated to Packaged System Environment ... 6

5.2.2 Unpackaged System Input Correlated to End User Use-Conditions ... 7

5.3 Test Recommendations ... 7

5.3.1 Testing Sample Recommendations ... 7

5.4 Test Flow ... 8

5.4.1 Packaged System Testing ... 8

5.4.2 Unpackaged System Testing ... 9

5.5 Post Test Analysis ... 9

5.6 Testing Output and Report Recommendations .. 10

5.6.1 General Considerations ... 10

5.6.2 Electrical Testing ... 10

5.6.3 Failure Analysis Considerations ... 10

5.6.4 Reporting Recommendations for Test Development ... 10

6 SYSTEM BOARD LEVEL TESTING ... 11

6.1 Board Testing Background ... 11

6.2 System Board Testing Recommendations ... 11

6.3 Correlation Criteria and Validity of Test Setup ... 11

6.4 Equipment Recommendations ... 11

6.5 Test Flows ... 11

6.6 Failure Analysis ... 12

6.7 Reporting Recommendations ... 12

7 COMPONENT MECHANICAL SHOCK ASSESSMENT ... 12

7.1 Component Assessment – General Considerations ... 12

7.2 Component Board Testing Recommendations ... 12

7.3 Correlation Criteria and Validity of Test Setup ... 13

7.4 Equipment Recommendations ... 13

7.5 Testing Flows ... 13

7.5.1 Characterization Testing ... 13

7.5.2 Qualification Testing ... 14

7.6 Failure Analysis ... 15

7.7 Reporting Recommendations ... 15

8 METRICS FOR MATCHING TEST ... 15

8.1.1 Acceleration Based Method ... 15

8.1.2 Board Strain Based Method ... 16

Annex A Sample Data Reporting Format ... 20

Annex B Metrologies ... 22

Annex C Shock Failure Analysis of Electronic Components ... 25

Annex D Suggestions for Selecting Sample Size ... 27

Annex E Suggestions for Finite Element Analysis in Mechanical Shock ... 29

Figures

Figure 4-1 Typical UCs where Mechanical Shock May be Expected for a Few Representative Products ... 3

Figure 5-1 Example of the Time History Response Showing the Input from the Shock Table (trapezoidal shape) and the Response at Two Locations on the PCB ... 7

Figure 5-2 Example of Shock Response Spectra (left) Derived from the Time History ... 8

Figure 6-1 Illustration of a Board Level Test on a Hard Plate ... 11

Figure 6-2 Illustration of a Board Level Test on a Rigid Fixture ... 12

Figure 6-3 Illustration of a Boundary Condition Simulator (BCS) ... 12

Figure 7-1 Flow Chart for Characterization Test ... 14

Figure 8-1 Basic Model for Board Level Testing (Assumes Worst Case Amplification and no other Interaction with Chassis) ... 16

Figure 8-2 Example of Correlation of a Board Test to Three Test Systems 17
Figure 8-3 Definition of Board Strain States Plot 17
Figure 8-4 Comparing Board Bend Modes of Board in System Chassis and Mounted to a Fixed Plate 18
Figure 8-5 Settling Time for a Typical System Level Test with High Damping and Rapid Decay in the Strain 18
Figure 8-6 Typical Time History for a Component Board Test with Minimal Damping 18
Figure B-1 Wire (a) Strain Gage Location with Respect to Solder Ball at Package Corner. (b) Orientation of Strain Gages for every Package Corner 22
Figure B-2 Wire Routing should be done So as Not to Affect Results 23
Figure B-3 Wire Artwork Showing Strain Gage Feature and Internal Board Routing 23
Figure B-4 Fast Fourier Transform of an Example System 23
Figure C-1 BGA Solder Joint Failure Modes 26
Figure C-2 Area Array Cross-Section Diagram 26
Figure E-1 Coarse Mesh of Plate 29
Figure E-2 Fine Mesh of Plate 29
Figure E-3 Rack Mounted Test Board 30
Figure E-4 Simplified Satellite Antenna Model 31
Figure E-5 Results for Simplified Satellite Antenna Model 32
Figure E-6 Comparison of Displacement-Time History for Experimental Data and FEA Result 37
Figure E-7 Comparison of Board Strain versus Time History for Experimental Data and FEA Result 37

Tables

Table 4-1 Example of a UC for a Mobile Phone, (Illustrative Only) 3
Table 7-1 Example of Critical Strain Determination Results. Value indicates number of drops at each level. (Shadows indicates electrical failure.) 14
Table 8-1 Recommended Matching Criteria for Selected Use and Test Conditions 16
Table A-1 Test Report Recommendations (Equipment and Materials) 20
Table A-2 Test Report Recommendations (Board Assembly) 20
Table A-3 Test Report Recommendations (Test Results) 21
Table B-1 Recommended Scan Frequencies for Various Systems 23
Table D-1 Sample Size Estimate for a Single Failure Mechanism 28
Table E-1 Full, Symmetric, and Asymmetric Meshes of Plate 30
Table E-2 Comparing Implicit and Explicit Dynamic Solutions 33

Mechanical Shock Test Guidelines for Solder Joint Reliability

FOREWORD

This publication has been drafted as part of a joint working group between the IPC 6-10d task group and the JEDEC JC14.1 subcommittee. It is intended to be used as a general guideline for mechanical drop and shock testing. It is also encouraged that future application specific mechanical shock standards and specifications for IPC and JEDEC should apply the methods proposed herein.

INTRODUCTION

With the growth of electronics and the increased accessibility and portability, drop shock and other mechanical impacts are increasingly a concern. This document attempts to improve upon past mechanical shock test methods, and tie test conditions back to the use-conditions. A method is proposed such that regardless of what level (system, board assembly, simplified single component board testing, etc.) testing is conducted, there should be a correlation back to the use-condition. In order to fulfill this goal, additional metrologies are introduced to aid in these correlations.

Following the requisite introductory sections, the concept of use-conditions is introduced and suggestions are made on how use-condition data may be acquired and applied. Next, the testing methods for fully assembled systems are introduced. Options for test conditions are discussed and the data that should be collected is outlined.

Testing of subassemblies and components mimics actual use configurations less than testing of fully assembled systems; however, the next two document sections outline considerations to ensure that testing done at these levels remains relevant to the intended use-condition.

Specific metrics to aid in correlations are outlined in Section 8. The informative annexes that close the document discuss *the* common considerations of all mechanical shock testing methods. These include a sample reporting format for test data, use and application of strain gages, accelerometers, and high speed photography. A section on failure analysis is given. Lastly, a review of finite element methods that may be applied to mechanical shock analysis is given to aid in more in-depth study of shock problems.

1 SCOPE

This document establishes mechanical shock test guidelines for assessing solder joint reliability of Printed Circuit Board (PCB) assemblies from system to component level.

The three main categories discussed within this document follow:

1. Methods to define mechanical shock use-conditions.
2. Methods to define system level, system board level and component test board level testing that correlate to the use-conditions.
3. Guidance on the use of experimental metrologies for mechanical shock tests.

2 APPLICABLE DOCUMENTS

2.1 IPC[1]

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-9252 Requirements for Electrical Testing of Unpopulated Printed Boards

2.2 American Society for Testing and Materials[2]

ASTM D3332 Standard Test Methods for Mechanical-Shock Fragility of Products, Using Shock Machines

3 TERMS AND DEFINITIONS

For the purposes of this document, the following terms and definitions apply:

Accelerometer An electronic device that converts mechanical deformation of an internal structure caused by acceleration into electrical signals that can be sensed by a data acquisition system.

Component Board Level Test A test conducted on a simplified test board which contains only one type of component, although multiple samples of the same component may be present. This board need not be similar to the final system board.

ODM Original design manufacturer.

OEM Original equipment manufacturer.

PWB Printed wiring board, also known as printed circuit board (PCB).

SRS A shock response spectrum is an analysis of the acceleration output signal into the frequency domain.

1. www.ipc.org
2. www.astm.org