IPC-TR-585

Time, Temperature and Humidity Stress of Final Board Finish Solderability

Developed by the Alternate Final Finishes Task Group (5-23d) of the Assembly & Joining Processes Committee (5-20) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois
60015-1219
Tel 847 615.7100
Fax 847 615.7105

Table of Contents

1 PURPOSE ... 1
2 INTRODUCTION ... 1
3 TASK OBJECTIVES ... 1
4 TEST PLAN ... 1
5 SAMPLE PREPARATION ... 2
6 SURFACE ANALYSIS OF SAMPLES ... 3
7 SAMPLE CONDITIONING (COUPON CONDITIONING) ... 4
8 SAMPLE TESTING ... 4
8.1 Wetting Balance Testing ... 4
8.2 Sequential Electrochemical Reduction Analysis (SERA) Testing ... 5
8.3 Dip and Look Testing ... 5
8.4 Wetting Balance Testing ... 5
8.5 SERA Testing ... 5
9 DATA ANALYSIS ... 7
9.1 Wetting Balance Results ... 7
9.2 Visual ... 8
10 CONCLUSIONS
10.1 Conclusions By Finish ... 8
10.1.1 Bare Copper ... 8
10.1.2 RTL ... 8
10.1.3 Immersion Silver ... 8
10.1.4 Immersion Tin ... 8
10.1.5 Electroless Nickel/Immersion Gold (ENIG) ... 8
10.1.6 OSP ... 9
10.2 Investigation Confirmation Testing ... 9
11 RECOMMENDATIONS ... 10
Appendix 1: Coupon Numbering System ... 11
Appendix 2 A: Charts for Reflowed Tin Lead ... 12
Appendix 2 B: Charts for Bare Copper ... 13
Appendix 2 C: Charts for Immersion Silver ... 14
Appendix 2 D: Charts for Immersion Tin ... 15
Appendix 2 E: Charts for Nickel Gold ... 16
Appendix 2 F: Charts for OSP ... 17
Appendix 3: Pareto Chart Analysis ... 18
Appendix 4: "Stop Light" Analyses of Wetting Balance Data ... 25
Appendix 5: Relative Stoplight and Box-and-Whisker Analysis of SERA Data ... 27
Appendix 6: Solderability Visual Exam ... 33
Appendix 7: Statement of Work for This Project at the Start ... 34
Appendix 8: IPC Dip and Look Test Method ... 39
Appendix 9: Further Analysis of the Alternate Final Finishes Task Group Report on Time, Temperature and Humidity Stress of Final Board Finish Solderability ... 41

Figures

Figure 4-1 Box Behnken Test Design ... 1
Figure 5-1 ENIG Coupons Before Plating ... 3
Figure 6-1 Cross Sections of Six "As Fabricated" Alternative Surface Finishes" ... 4
Figure 7-1 Immersion Silver Coupons ater Conditioning ... 4
Figure 8-1 Alternative Surface Finishes after Dip and Look Solderability Testing ... 6
Figure 8-2 Cross Section of Alternative Surface Finish Coupons After Dip and Look Solderability Testing ... 6
Figure 8-3 Schematic of SERA Apparatus ... 7
Figure 8-4 Typical SERA Plot ... 7
Figure 9-1 Sample Box and Whisker Plot from Data Taken from Reflowed Tin Lead ... 8
Figure 10-1 Results from Gold Thickness Survey of IPC 4-14 Subcommittee that wrote IPC-4552 ... 9
Figure 10-2 Wetting Balance Coupon (FR-4, 0.062 in thick, acid copper plated, six 3 mm SMD pads/side) ... 9
Figure 10-3 Confirmation Run 8 Hour Test Results ... 9
Figure 10-4 Confirmation Run 24 Hour Test Results ... 10

Tables

Table 4-1 Test Plan ... 2
Table 5-1 Coupons and Sources ... 2
Table 6-1 Comparison of XRF and Auger Measurements ... 3
Table 8-1 Oxide Reduction Potentials ... 7
Table 8-2 Oxide Thickness Calculation ... 7
Table 10-1 Means and Standard Deviations for Figure 10-1 ... 9

Time, Temperature and Humidity Stress of Final Board Finish Solderability

1 PURPOSE

The purpose of this investigation is to identify a stress test that will distinguish between robust and non-robust finishes. A robust finish will pass a test for solderability, and a non robust finish will fail. The stress test need not duplicate real world environment (fabrication through assembly), but it must correlate to solderability performance.

2 INTRODUCTION

The IPC 5-23d - Alternate Final Board Finishes Task Group is organized under the IPC Assembly and Joining Committee. Alternate Final Board Finishes Task Group activity began in the mid 1990s under IPC 5-23 Solderability Subcommittee. Surface mount technology was rapidly replacing through-hole construction. Planar surfaces, better than reflowed solder or hot-air-solder-level (HASL), were required. Originally, IPC standards for solderability testing were written around tin/lead surfaces only. It was proposed by committee participants that a whole new standard would be needed for testing the solderability of these new final board finishes.

Adjustments to the J-STD-003 specification allowed for the testing of board finishes other than tin lead. Therefore, committee attention turned to the measurement of stress effects of temperature, humidity, and time on alternative board finishes as measured by a variety of test methods. In addition, the committee tested the finishes with a promising newer technique - Sequential Electrochemical Reduction Analysis (SERA).

The potential exists to use this stress test data as a quality control tool and, perhaps, with correlation to observed individual situation data - to serve as a guideline for board storage or shelf life.

As board assembly facilities are located in various climate conditions, and board storage varies from company to company, no general guidelines can be given. However, to correlate to individual company conditions, a better understanding of alternate finish response to stress can be useful in product planning and supply chain management.

3 TASK OBJECTIVES

The objective of this test program is to determine a relationship between the three environmental stress conditions - temperature, moisture, and time - and the solderability of four alternate final board finishes. Two baseline conditions were used for comparison:

- Reflowed tin/lead electroplate (RTL)
- Bare copper (BC) - sometimes called ‘‘nude’’ copper referring to the ‘‘as plated’’ condition, not the ‘‘bare copper’’ of foil on circuit boards in shipment.

Four alternate finishes were selected - all of which have been used to assemble circuit boards for several years now.

- Organic solderability preservative (OSP)
- Immersion Silver (IS)
- Immersion Tin (IT)
- Electroless Nickel/Immersion Gold (ENIG - within this report the designation NG may be used)

Also the committee is trying to develop a model which can be used to:

- Determine screening test conditions to assess board solderability during production.
- Evaluate solderability process capability for five given surface finishes, plus bare copper baseline.
- Develop a method to evaluate potential new alternative surface finishes and compare predicted solderability performance to current finishes (terminology such as ‘‘aging’’ is not used in deference to ‘‘stressing’’). For example ‘‘steam stressing’’ is preferred to ‘‘steam aging’’).

4 TEST PLAN

A test plan was developed in order to investigate various surface stresses on surface finishes. This test plan evolved into a designed experiment approach that allowed investigation of many factors with minimal experimentation. The DOE design was a Box Behnken model (Figure 4-1).

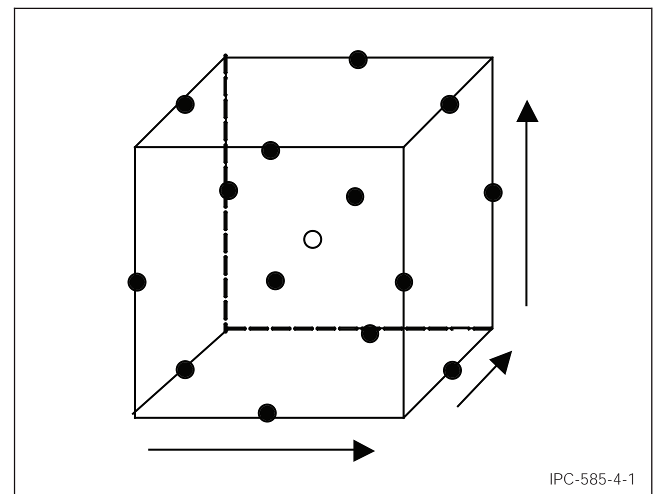

Figure 4-1 Box Behnken Test Design