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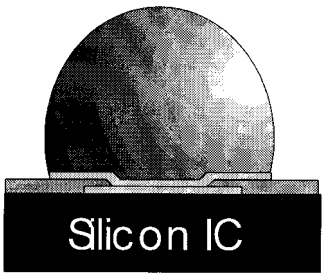

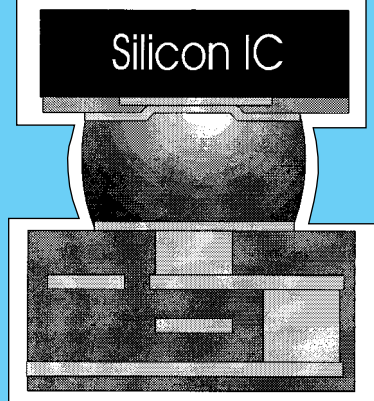

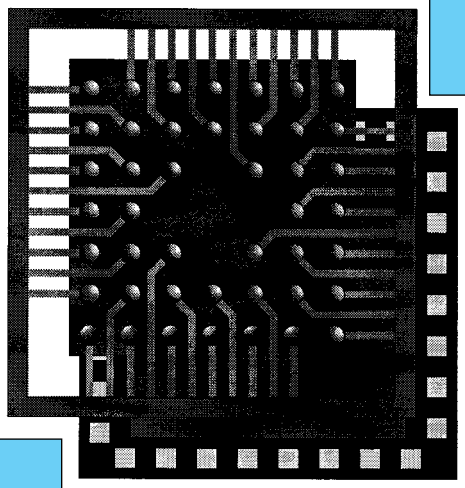

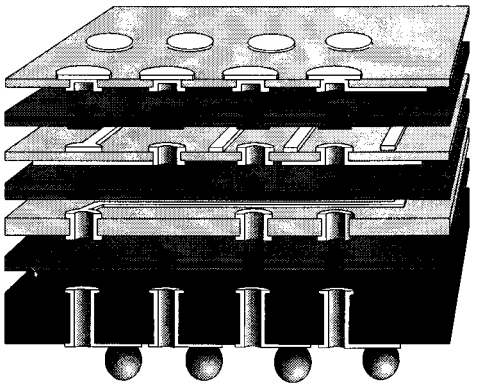

JOINT INDUSTRY STANDARD

IMPLEMENTATION OF FLIP CHIP AND CHIP SCALE TECHNOLOGY

COORDINATED BY THE SURFACE MOUNT COUNCIL

EIA ELECTRONIC INDUSTRIES ASSOCIATION EST. 1924

IPC

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Table of Contents

Figures

Tables

Implementation of Flip Chip and Chip Scale Technology

1 SCOPE

This document describes the implementation of flip chip and related chip scale semiconductor packaging technologies. The areas discussed include: design considerations, assembly processes, technology choices, application, and reliability data. Chip scale packaging variations include: flip chip, High Density Interconnect (HDI), Micro Ball Grid Array (μBGA), Micro Surface Mount Technology (MSMT) and Slightly Larger than Integrated Circuit Carrier (SLICC).

1.1 Purpose

This document is intended to provide general information on implementing flip chip and chip scale technologies for creating single chip or multichip modules (MCM), IC cards, memory cards and very dense surface mount assemblies.

1.2 Categorization

Flip chip is categorized as versions of a tin-lead (SnPb) solder bump process, and alternative solutions that use other forms of chip bond site bumping.

Chip scale technology is categorized as semiconductor chip structures that have been made robust to facilitate ease of chip handling, testing and chip assembly. The chip scale technologies have common attributes of minimal size, no more than 1.2X the area of the original die size, and are direct surface mountable.

2 TECHNOLOGY OVERVIEW

Flip chip and chip scale technology relate to methods used to provide an efficient technique for interconnecting semiconductor die to a substrate. Over the years flip chip technology has grown in stature and expanded into the more generic area of chip scale technology. In addition, many new techniques for mounting bare die were also established. Today, enhancements of the semiconductor die, which ruggedize the product to facilitate ease of handling and testing, have established another level of packaging technology in which many companies can participate.

2.1 History of Flip Chip

Flip chip solder bump interconnection technology is over 30 years old. It was first conceived and developed in 1960-61 by IBM for the Solid Logic Technology (SLT) hybrid electronic circuitry in IBM's System 360 computers introduced in April 1964.

At that time, standard transistor packaging used hermetically sealed metal cans with glass sealed wires emerging from a header upon which the germanium or silicon chip was metallurgically backbonded. Manual thermocompression wire bonding to the chip was the common technique.

Although transistor technology was much more reliable than vacuum tube technology that preceded it, the packaging and interconnection technologies were weak. Faulty manual wire bonds, purple plague (gold-aluminum intermetallic formation), and aluminum corrosion of thin film interconnections on the chip, even in hermetic packages, were all reliability concerns. In addition, manufacturability and productivity were deficient.

SLT transistors and diodes were glass passivated at the wafer level to protect aluminum wiring from the environment. Glass frits of borosilicate glass were fused on the surface of transistor wafers after the aluminum wiring was formed. The glass film obviated the need for a hermetic enclosure because the transistor was sealed at the chip level.

Consistent with maintaining a hermetic seal was the idea of etching via holes in the glass where electrical connections were to be made, and hermetically resealing the holes with an overlapping, larger pad of metal films. The first film, typically chromium, was used to create a good bond to glass and aluminum.

Subsequent metal films, typically copper and gold, were deposited to provide wettability and solderability for a ball of metal alloy that was to be melted on the pad. Originally, the ball was an alloy of Au-Sn eutectic which melted at 360°C; therefore, the pad was called the ball-limiting metallurgy because the melted ball would not wet the glass beyond the area of the pad. Later the ball or bump became a solder bump with an embedded copper ball ''stand-off,'' shown in figure 2-1.

The packaging concept required that thick film electrodes or wires be screened and fired on alumina substrates. Originally, the thick film was glass fritted Au-Pt paste; later it became Ag-Pd. The wiring was hot dip tinned with 90Pb-10Sn solder to improve conductance and to interconnect the active and passive components. For each transistor, three of the screened wires were to terminate in a spot that would be the mirror image of the chip bumps.

After each chip site was fluxed with a droplet of sticky water white rosin flux, the chip was picked up and placed on the solder coated electrodes face down or ''flipped'' compared to normal chip placement. Subsequently, the substrate was heated in a furnace to remelt the solder coating,