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J-STD-027

Mechanical Outline Standard for Flip Chip and Chip Size Configurations

About This Document

This document is intended to report on the work being done by several organizations concerned with the design of bare die in flip chip or chip scale configurations. Details were developed by companies who have implemented the processes described herein and have agreed to share their experiences. Readers are encouraged to communicate to the appropriate trade associations or societies any comments or observations regarding details published in this document, or ideas for additional details that would serve the industry.

Users of this standard are encouraged to participate in the development of future revisions.

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Mechanical Outline Standard for Flip Chip and Chip Size Configurations

1 SCOPE

This standard establishes mechanical outline requirements for devices supplied in flip chip or Chip Size Package (CSP) formats, including die surface, die terminals, and interconnection balls/bumps/lands to the next level.

1.1 Purpose The purpose of this standard is to establish a family of mechanical outlines and footprints for both the device and the interconnection scheme. Interconnection ball/bump/land size, pitch, configuration, coplanarity, and associated tolerances are included in this standard.

1.2 Intent The intent of this standard is to minimize the number of variations for the mechanical configurations, so a family of substrates and die/CSP-level test and burn-in socket can be manufactured at high volume for low cost consumption.

2 APPLICABLE DOCUMENTS

J-STD-012 Implementation of Flip Chip and Chip Scale Technology, January 1996

J-STD-026 Semiconductor Design Standard for Flip Chip Applications

IPC-SM-782 Surface Mount Design and Land Pattern Standard

JEDEC Publication 95 Semiconductors Design Guides and Package Outlines

JEDEC Standard 95-1 Section 5 Fine Pitch Ball Grid Array Packages (FBGA) Square Design Guidelines

JEDEC Standard 95-1 Section 6 Fine Pitch Ball Grid Array Packages (FBGA) Rectangular Design Guidelines

JEDEC Standard 95-1 Section 14 Ball Grid Array Square and Rectangular Design Guidelines

3 REQUIREMENTS

3.1 Recommended Mechanical Outline for Flip Chip Dice and Chip Size Packages Flip chip dice and wafer level chip size packages are designed as a part of the fundamental device design. They provide the designer with wide latitude in the mechanical outline, function, and performance of the produced product. The designer's choice of mechanical outline can affect the ease of handling and assembly of the part when it is attached to the substrate.

Standardized mechanical outlines and design guides can be found in JEDEC Pub 95. These standards have led to standardized supplies of tape, component feeders, and second sources. It is recommended that the design of flip chip and wafer level CSPs adapt these outlines to minimize the extra work and expense that may be incurred to use a nonstandard outline.

It is also recommended that the interconnection ball/bump/land patterns for full area array flip chip and CSP devices be standardized to minimize extra work and expense for test, burn-in, and handling. The proposed configurations will be discussed in the Interconnection Patterns section.

3.1.1 Flip Chip Devices The dimensions of flip chip dice are determined mainly by the design and wafer processing, and is therefore difficult to impose standards. However, the standardization of the interconnection pattern will reduce the costs for Known Good Die (KGD), die test, burn-in, and handling. Recommended footprints would use standard pitches and an appropriate grid for the interconnect attributes.

3.1.2 Chip Size Packages There are various pitches that impact the characteristics of the balls/bumps/lands and the number of each of the conditions that exist. In order to determine the relationships between number of balls and chip size, the characteristics of the different pitches are noted in Table 1.