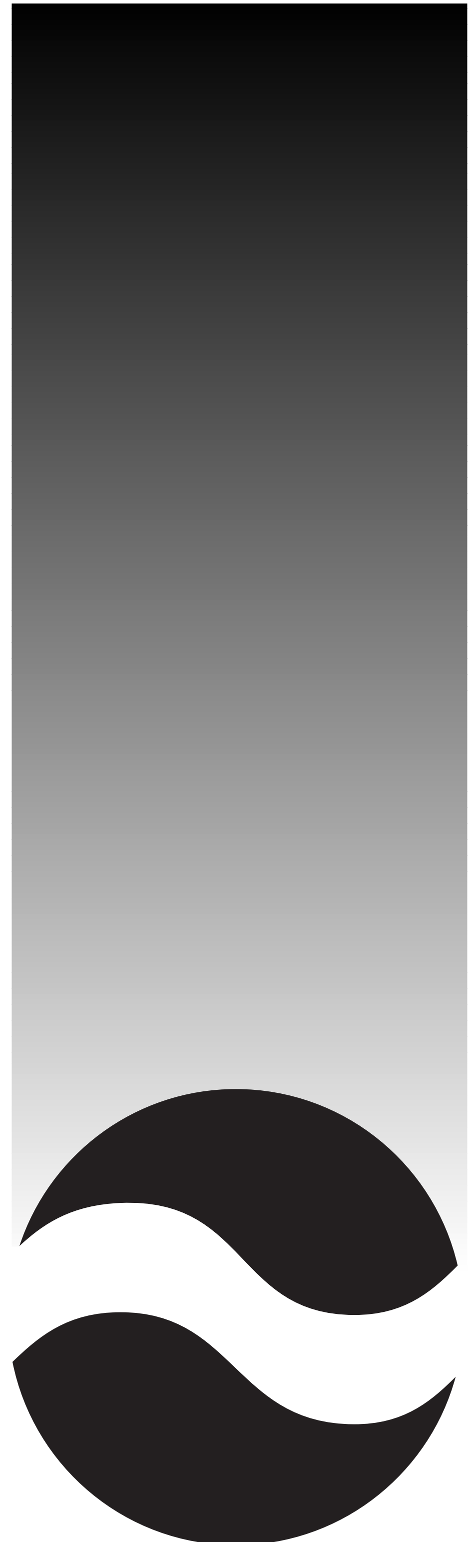
IPC/EIA J-STD-028
AUGUST 1999

JOINT INDUSTRY STANDARD

Performance Standard for Construction of Flip Chip and Chip Scale Bumps



IPC/EIA J-STD-028

Performance Standard for Construction of Flip Chip and Chip Scale Bumps

About This Document

This document is intended to report on the work being done by several organizations concerned with the design of bare die in flip chip or chip scale configurations. Details were developed by companies who have implemented the processes described herein and have agreed to share their experiences. Readers are encouraged to communicate to the appropriate trade associations or societies any comments or observations regarding details published in this document, or ideas for additional details that would serve the industry.

Users of this standard are encouraged to participate in the development of future revisions.

Contact:

EIA
Engineering Department
2500 Wilson Boulevard
Arlington, VA 22201
Phone (703) 907-7500
Fax (703) 907-7501

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Phone (847) 509-9700
Fax (847) 509-9798

Table of Contents

1 SCOPE 1
1.1 Purpose 1
1.2 Intent 1
1.3 Presentation 1
1.4 Interpretation 1
1.5 Organization of Design Information 1
1.6 Order of Precedence 1

2 APPLICABLE DOCUMENTS 1

3 REQUIREMENTS 2
3.1 Terms and Definitions 2
3.2 General Performance Requirements 2
3.2.1 Bump and Joint Expectations 2
3.3 Classes of Flip Chip Joints 2
3.4 Meltable Solder Bump Process 3
3.4.1 Solder Evaporation Process (see 4.1) 3
3.4.2 Solder Electroplating Process (see 4.2) 3
3.4.3 Solder Paste Deposition Process (see 4.3) 4
3.4.3.1 Solder Screen Printing Process 5
3.4.3.2 Stencil Transfer Process 5
3.4.4 Non-Noble Metal Bump Material Issues 5
3.4.5 Indium-Based Bumps for Chip-on-Glass Attachment 6
3.5 Partially Meltable Bump Process (see 4.4 and 4.5) 6
3.6 Non-Meltable Bumps Process (see 4.6, 4.7 and 4.8) 6
3.6.1 Gold Bump Material Issues 6
3.7 Polymeric/Conductive Adhesive Bump Processes (see 4.9) 6
3.7.1 Design Issues 6
3.7.2 Conductive Paste Method 7
3.7.3 Conductive Adhesives Process 7
3.7.3.1 Anisotropic Adhesive Details 8
3.7.4 Gold Bump Adhesive Material Issues 8
3.8 Bump Mechanical Requirements 9
3.8.1 Diameter, Volume, Height Uniformity 10
3.8.2 Bump Strength 10
3.8.2.1 Pull Test and Fracture Mode 10
3.8.2.2 Shear Test 11
3.9 Electrical Parameters 11
3.9.1 Bump Resistance 11
3.9.2 Inter-Bump Surface Insulation Resistance (Leakage) 11
3.9.3 Current Carrying Capability 11
3.9.4 Bump Stress Effects on Underlying Devices and Conductors 11
3.10 Metallurgical/Chemical Requirements 11
3.10.1 Metallurgical Composition 11
3.10.1.1 Alloying Materials and Tolerances 12
3.10.1.2 Bulk Contaminants and Inclusions 12
3.10.2 Alpha Particle Emission 12
3.10.3 Solderability 13
3.10.3.1 Wettability 13
3.10.3.2 Melting Point 13
3.10.4 UBM Integrity 13
3.10.4.1 Adhesion 13
3.10.4.2 Liquid Metal 14
3.10.4.3 Stress Induced Failure Modes 14
3.11 Mounting Substrate Surface Finishes 14
3.11.1 Metallic Surface Finish Materials 14
3.11.2 Organic Protective Coating Materials 15

4 CONSTRUCTION DETAIL STANDARD FOR FLIP CHIP BUMPS 15
4.1 Totally Meltable Evaporated Bump 15
4.2 Totally Meltable Electroplated Bump 16
4.2.1 Typical Electronic Electroplated Bump 16
4.2.2 Typical Electroplated Bump 18
4.3 Totally Meltable Solder Paste Deposition 19
4.4 Partially Meltable Bump (Cu Stud Base) 20
4.5 Partially Meltable Bump (Pb Stud Base) 20
4.6 Non-Melting Bumps (Au Electroplated) 21
4.7 Polymeric/Conductive (Conductive Bump with Isotropic Adhesive) Adhesive Bumps 22

Annex A Normative Terminology and Acronyms 23

Annex B Acronyms 25

Figures

Figure 1 Plated Solder Pads 4
Figure 2 Reflowed Solder Bumps 4
Figure 3 An example of Fine Line Stencil Printing 5
Figure 4 Chip on Glass Technology 6
Figure 5 Gold Bumped IC Adhesively Attached to a Glass Substrate 8
Figure 6 Cross-Section View of Chip on Glass Connection 9
Figure 7 Bump Electrical Path (Redistributed Chip) 10
Figure 8 Alpha Particle Emission Track and E/H Pairs 12

Figure 9 Distortion of Depletion by Alpha Particles 13
Figure 10 Layout of Solder Paste Deposition (FOC) Bump Pad 14
Figure 11 Solder Bump Vertical Cross Section 15
Figure 12 Typical Electronics Electroplated Bump 17
Figure 13 Solder Bump Cross Section 18
Figure 14 Flip Chip Technologies Solder Bump Cross-Section 19
Figure 15 Partially Meltable E-3 Bump Cross Section 20
Figure 16 Gold Bump Cross Section 21
Figure 17 Epoxy Technology Isotropic Conductive Adhesive Bump 22

Tables

Table 1 Alpha Particle Emissions of Semiconductor Materials 13
Table 2 Totally Meltable Solder Joints: High Pb based Pb Sn (evaporated type) Data for Bump Diameter /Pitch: 125 µm/250 µm (other bump sizes & pitches scaleable) 16
Table 3 Totally Meltable Solder Joints: Sn-Pb, Eutectic or High Pb (Unitive Electronics Inc. Electroplated type) Data for Bump Diameter /Pitch: 125 µm/250 µm (other bump sizes & pitches scaleable) 17
Table 4 Totally Meltable Solder Joints: Sn-Pb, Eutectic or High Pb (Aptos Electroplated type) Data for Bump Diameter /Pitch: 100 µm/200 µm (other bump sizes & pitches scaleable) 18
Table 5 Totally Meltable Solder Joints: Eutectic based Pb/Sn (Delco/Flip Chip Technologies Paste Deposition type) Data for Bump Diameter /Pitch: 152 µm/250 µm (other bump sizes & pitches scaleable) 19
Table 6 Partially Meltable Solder Joints: High Pb based Pb Sn (Motorola evaporated type) Data for Bump Diameter /Pitch: 150 µm/300 µm (other bump sizes & pitches scaleable) 20
Table 7 Non-melting Bump: Gold (Aptos Electroplated type) Data for Bump Diameter /Pitch: 50 µm/80 µm (other bump sizes & pitches scaleable) 21
Table 8 Polymeric/conductive-conductive bump with isotropic adhesive (Epoxy Technology Adhesive Bumps) Data for Bump Diameter /Pitch: 150 µm/300 µm (other bump sizes & pitches scaleable) 22

Performance Standard for Construction of Flip Chip and Chip Scale Bumps

1 SCOPE

This standard establishes the construction detail requirements for bumps and other terminal structures on flip chips and chip scale carriers. All flip chip and chip scale device terminals shall meet the designated standards detailed in this document which includes such diverse terminations as solder bumps, columns, non-melting stand-offs and conductive polymer deposits. The specific standards for different terminations will therefore be appropriately matched to the particular interconnection.

1.1 Purpose The purpose of this document is to establish a set of designations and expectations for product performance for the manufacturer and user of flip chip or chip scale devices. Included in this will be the flexibility to implement the best commercial practices and evolving improvements on those practices.

1.2 Intent The intent is to recognize a large variety of terminal structures for a wide range of applications ranging from highest reliability computer, space and military applications to disposable commodity applications. Subsections in this document will provide for the flexibility to meet the cost and performance requirements.

1.3 Presentation All dimensions and tolerances in this standard are expressed in metric units with millimeters being the main form of dimensional expression. Inches may be shown in brackets as appropriate and are not always a direct conversion depending on the round-off or the required precision. Users are cautioned to employ a single dimensioning system, and not intermix millimeters and inches. Reference information is shown in parentheses ( ).

1.4 Interpretation **Shall**, the emphatic form of the verb, is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a **shall** requirement may be considered if sufficient data is supplied to justify the exception.

The words *should* and *may* are used whenever it is necessary to express non-mandatory provision.

Will, is used to express a declaration of purpose.

To assist the reader, the word **shall** is presented in bold characters.

1.5 Organization of Design Information This standard is organized into various sections in order to provide information for the design of flip chip devices. The main sections with their points of emphasis are:

Section 3 Design Considerations
Section 4 Quality Assessments

1.6 Order of Precedence In the event of any conflict in the development of new designs, the following order or precedence should prevail:

1. The customer requirements.
2. Substrate design rules.
3. Bump design rules.
4. This standard.

2 APPLICABLE DOCUMENTS

The following documents contain provisions which, through reference in this text, constitute a part of the J-STD-028. At the time of publication, the editions indicated were valid. All documents are subject to revision and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions.